REMARKS

This Response is submitted in reply to the Non-final Office Action mailed June 16, 2005. Claims 10-18 are hereby cancelled, and new claims 19-23 are hereby added. Claim 19 is in independent form. No new matter has been added.

The Commissioner is hereby authorized to charge any fees which may be required in the Application to Deposit Account No. 02-1818. Please reference number 112740-190 if such a withdrawal is made.

Specification

The Office Action objected to the Abstract because it was not displayed on a separate page. Please amend the specification by moving the Abstract to a separate page following the last page of the claims.

Claim rejections under 35 U.S.C. §102(e)

The previously pending claims (claims 10-18) were rejected under 35 U.S.C. §102(e) as being anticipated by Nakano (U.S. 6,011,787). In light of the amendments made herein, applicants respectfully traverse these rejections. Favorable reconsideration is respectfully requested.

Applicant fails to see where Nakano teaches a pipelined architecture in a rake receiver. In order to further this distinction, Claim 19 replaces claim 10 in order to clarify the structure and operation of the three pipeline stages in the present invention. As currently presented, Claim 19 (the only independent claim) distinguishes the prior art of record, including Nakano.

Specifically, Claim 19 recites a rake receiver with "a pipeline architecture including three pipeline stages." The first pipeline stage includes "a memory device". The first pipeline stage "reads received chips from the memory device and calculates an address by adding a value of a free running address counter to at least one rake-finger dependant offset". The second pipeline stage includes an "interpolator" to "determine conjugate complex coefficients by interpolating between two channel estimations". The third pipeline stage includes "an accumulator" to "provide early/late tracking of the rake fingers". In addition, claim 19 recites "registers" for "buffering data between the pipeline stages".

No prior art reference of record teaches this combination. In particular, Nakano fails to

teach the structural features of the pipeline stages as recited in new claim 19. Nakano does discuss a rake receiver. However, Nakano does not discuss a pipelined architecture as currently claimed. Instead, Nakano merely teaches a "delay circuit 42 [that] applies different delays for different sectors so that the communication channels of different sectors are displaced" (col. 16, lines 9-11). In this manner, "even when the transmission is carried out simultaneously from a plurality of sectors, the signals from different sectors do not overlap at any timing, so that the reception paths are separated and the characteristic of the RAKE receiver can be improved (col. 17, lines 7-11).

Conclusion

In light of the above amendments and remarks, Applicant submits that all claims are in condition for allowance and request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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